REMARKS

Claims 1-10 are presented for examination. The Examiner has withdrawn his rejections of the claims under 35 U.S.C. 112, second paragraph, and objections to the drawings.

Claims 1-10 stand rejected under 35 U.S.C. 102(e) as being anticipated by Ho.

This rejection is respectfully traversed for the following reasons.

The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312, 197 USPQ 5 (CCPA 1978).

As demonstrated below, Ho does not disclose the apparatus or method substantially identical with the claimed invention.

In particular, claim 1 recites a back annotation apparatus including:

-a pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit;

-a layout pattern verification implementing part for implementing a predetermined layout pattern verification for layout patterns of said logical circuit;

-a parasitic element extraction part connected to said pre-layout simulation implementing part which extracts parasitic elements from said nodes of which the potential changes;

-a net list generation part connected to said parasitic element extraction part for generating a net list which includes all the devices included in said layout pattern data and parasitic elements extracted in said parasitic element extraction part; and

-a post layout simulation implementing part connected to said net list generation part for implementing a post layout simulation by using said net list.

Claim 6 recites the respective steps including:

-the step of detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit;

-the step of implementing a predetermined layout pattern verification with respect to a layout pattern of said logic circuit;

-the step of extracting parasitic elements from said nodes of which the potential changes;

-the step of generation of a net list including all the devices included in said layout pattern data and the parasitic elements extracted in said step of extracting parasitic elements; and

-the step of implementation of a post layout simulation by using said net list.

In the previous Response, Applicant submitted that Ho does not teach the pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as claim 1 requires; or the step of detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as recited in claim 6.

In response, the Examiner has taken the position that Ho teaches a continuous net by net extraction that includes extracting node information after or before a potential change occurs at the node. The Examiner relies upon col. 5, lines 1-6 and 15-20 of the reference.

Considering the reference, Ho discloses a layout parasitic extraction system that involves Net-by-net R and C Extract 111 that extracts layout parasitics net by net (col.5, lines 3-5). However, Ho does not suggest pre-layout simulation for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as claims 1 and 6 require.

Hence, Ho does not expressly disclose the pre-layout simulation implementing part of claim 1 and the respective step of claim 6.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

However, as demonstrated below, one skilled in the art would realize that pre-layout simulation implementing part of claim 1 and the respective step of claim 6 are not present in the layout parasitic extraction system of Ho.

Ho discloses that the Net-by-net R and C Extract process 111 is performed after Conversion 101, which is the first step in the method of Ho, and "which generates a connectivity-based database file where geometries of the layout are referenced according to the

circuit schematic by net." (col. 4, lines 24-26). Hence, the Conversion 101 and the Net-by-net R and C Extract 111 are carried out after the layout is created.

Therefore, the steps 101 and 111 of Ho can not be pre-layout simulation steps.

It is noted that the Examiner has apparently failed to give adequate consideration to the particular problems and solution addressed by the claimed invention. ***Northern Telecom, Inc. v. Datapoint Corp.***, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); ***In re Rothermel***, 276 F.2d 393, 125 USPQ 328 (CCPA 1960).

As discussed in the specification, in accordance with a conventional back annotation approach, after a layout is completed, parasitic elements are extracted from the layout and a post-layout simulation is performed. The claimed invention addresses problems of reducing time required for parasitic element extraction and simplifying the post-layout simulation.

These problems are solved by introducing a pre-layout simulation to detect nodes of which the potential changes when a predetermined signal is applied to a logic circuit.

Ho does not address the problems and solutions addressed by the claimed invention.

As Ho neither expressly nor inherently discloses the pre-layout simulation implementing part of claim 1 and the respective step of claim 6, the reference does not anticipate the claimed invention within the meaning of 35 U.S.C. 102. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

Hence, the rejection of claims 1-10 as being anticipated by Ho is not warranted.

In view of the foregoing, and in summary, claims 1-10 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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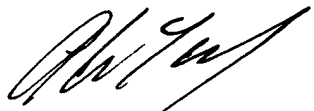

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